Amendments to the Specification:

Please replace paragraph [0039] with the following amended paragraph:

[0039] FIG. 4 illustrates an electronic system 402 in which configuration data from each of the devices 404-1 – 404-*n* in the system may be used to identify the system. Certain PLDs, such as various FPGAs from XILINX ~~Xilinx~~, Inc., may be connected in serial for loading and reading back configuration data. The devices have pins for input of configuration bits. For example an input pin of device 404-1 is connected to line 406. Similarly, the devices have output pins for output of configuration bits. For example, a configuration output pin of device 404-*n* is connected to line 408. The configuration bits and boundary-scan bits may use the same pins for input of data, as illustrated. In other implementations, the configuration bits and scan bits may be input on separate pins.